a second integrated circuit chip secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip;

a chip insulating layer disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material and a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material.

2. (Amended) The semiconductor structure of Claim 1 further comprises a conductor insulating layer formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material and a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the dielectric constant of the conductor insulating layer is lower than the dielectric constant of the insulating material.

19. (Amended) A multichip cube structure having a plurality of integrated circuit chips, comprising:

a first integrated circuit chip having a first insulating layer disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant, wherein at least a portion of the first insulating layer contains enclosed regions of air, wherein the dielectric constant of the first insulating layer is lower than the first dielectric constant;

a second integrated circuit chip secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;

a second insulating layer disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant, wherein at least a portion of the second insulating layer contains a plurality of enclosed regions of air, wherein the dielectric constant of the second insulating layer is lower than the second dielectric constant.